Notice of Allowability	Application No.	Applicant(s)	
	10/809,733	AVAKIAN ET AL.	
	Examiner	Art Unit	
	Shawn Gu	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the application filed on 3/25/2004 and the telephone interview on 25 May 2006*.

2. ☒ The allowed claim(s) is/are *1-3*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *03052006* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. This Office action is in response to the application filed on 25 March 2004. Claims 1-3 have been allowed.

Examiner's Amendment

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in telephone interviews with Richard Sharkansky (REG #: 25,800) on 5 May 2006 and 25 May 2006.

3. Amendments in claim 1:

on line 11, change "in to" to "into";

on line 13, change "device" to "devices".

4. Amendments in claim 2:

on line 1, change "in claim 2" to "in claim 1";

on line 2, change "the training request signal" to "a training request signal";

on line 4, change "setting a delay applying the read strobe pulses" to "applying a delay to the read strobe pulses";

on line 13, change "in accordance a predetermined" to "in accordance with a predetermined".

5. Amendments in claim 3:

on line 7, change "processing the user data" to "processing user data";

on line 9, change "setting a delay" to "applying a delay";

on line 16, change "until" to "for";

on line 19, change "in" to "and";

on line 20, change "the user data" to "user data".

Statement of Reasons for Allowance

6. The following is an examiner's statement of reasons for allowance:

The cited reference Magro et al. [US 6,889,334 B1] teaches reiteratively testing the latency of a test data strobe to generate a different delay value for each memory (Col. 12, Ln. 28-33), the testing is performed for each memory individually by incrementally adding delay values until a corresponding desired result is achieved (see Fig 9, Col. 10, Ln. 31-67, Col. 11, Ln. 1-8).

Janzen et al. [US 6,658,523 B2] teaches testing and adjusting read latencies of a plurality of memories by finding the largest value among the latency values experienced by the memories, and offsetting each memory's read latency so that all memories experience the same read latency (see Abstract, and Col. 6, Ln. 20-40). Instead of a single delay value, different delay values (offset values) are applied (added to the inherent read latencies) to each memory according to the reference.

Libby et al. [US 6,941,433 B1] teaches testing and finding the actual read latency of a single memory, the determined latency being smaller than the assumed worst case delay, in order to improve the read access capabilities of a data processing system (see Col. 1, Ln. 38-48).

Lee et al. [US 6,735, 709 B1] teaches calibrating a signal to a plurality of memory banks by iteratively applying a predetermined number of delay values in order to determine the optimal delay value for the signal (see Col. 9, Ln 48-67; Col. 10, Ln. 1-33, 60-67; Col. 11, Ln. 1-19, 50-56). However, the calibration is performed on only one signal associated to the memory banks (there is only one DQ or CMD/ADDR signal associated with all memory banks, see Fig. 2), not to a plurality of signals each of which is associated with a memory bank as indicated by claims 1 and 3. The delay values applied to CMD/ADDR and DQ of a particular DRAM 11 and the delay values applied to all DQ or CMD/ADDR signals of all DRAMs 11a-n are not the same value as required

by claims 1 and 3. Instead, the calibrated delay is added to only one particular signal such as DQ or CMD/ADDR of a particular DRAM 11.

Avakian et al. [US 7,016,240 B1] fails to claim the same limitations as taught by claim 1 of the instant application. Specifically, Avakian et al. ('240) does not claim "such delay being applied into the plurality of read strobe pulses to enable valid read data from the plurality of memory chips ..." as stated in paragraph (c) of claim 1 of the instant application, and "delaying the plurality of read strobe pulses by the determined read strobe pulse ..." as stated in paragraph (d) of claim 1 of the instant application. Avakian et al. ('240) only claims "using" the determined read strobe pulse delay, for subsequent reads.

None of the cited references above teaches the limitation in Claim 1, paragraph (c), which states "determine the read strobe pulse delay, such delay being applied into the plurality of read strobe pulses to ... in response to the read strobe pulses being delayed by the read strobe pulse delay". This limitation specifically indicates applying a single determined delay value to all read strobe pulses in order to provide valid read data from a plurality of memory chips.

None of the cited references teach the limitations in Claim 3, paragraphs (b), (d) and (g)-(j), which as a group teach iteratively testing each delay value in a set of delay values, and determining a single delay value to be applied to all read strobe pulses associated with a plurality of memory chips.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Gu whose telephone number is (571) 272-0703. The examiner can normally be reached on 9am-5pm, Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shawn X Gu
Patent Examiner
Art Unit 2189

25 May 2006

REGINALD G. BRAGDON
PRIMARY EXAMINER